



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/041,062	12/28/2001	Edward T. Grochowski	42390P13774	1970

7590 03/01/2005

Leo V. Novakoski
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER

PHAN, THAI Q

ART UNIT

PAPER NUMBER

2128

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/041,062	GROCHOWSKI ET AL.	
	Examiner	Art Unit	
	Thai Q. Phan	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 December 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-25 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 15-21 is/are allowed.
- 6) ☒ Claim(s) 1-14 and 22-25 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date: _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

JR

DETAILED ACTION

This Office Action is in response to patent application S/N: 10/041,062, filed on 12/28/01. Claims 1-25 are pending in the present action.

Drawings

The drawings filed on 12/28/2001 are acceptable for examination.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 and 22-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Linda Hurd, US patent no. 6,125,334.

As per claim 1, Hurd anticipates a method and system for determining the power consumption of an integrated circuit with feature limitations very identical to the claimed invention. According to Hurd, the simulation method includes steps

Simulating an operation of the device over a sequence of intervals (col. 7, line 16 to col. 10, line 37),

Determining an activity profile for the device from current drawn by the device in each of the intervals (cols. 10-12),

Art Unit: 2128

Determining response of the power network by applying pulse or impulse stimulus to the network (col. 10, lines 1-25),

And filtering the activity profile with the impulse response of the power delivery network to provide a profile of the voltages at the device (cols. 10-11).

As per claim 2, Hurd anticipates the device being simulated is a processor, and simulating the device operation for a series of instructions over a sequence of clock intervals (cols. 8-10).

As per claim 3, Hurd anticipates power consumption due to active and idle currents as claimed.

As per claim 4, Hurd anticipates the activity profile and an FIR filter for calculation of system response as claimed (col. 10, lines 1-37).

As per claim 5, Hurd anticipates a power consumption profile for the device under execution of a sequence of simulated instructions (Summary of the Invention, cols. 10-12).

As per claim 6, Hurd anticipates a processor under simulation and current consumption is determined by summing active and idle currents for clock gated units of the processor in response to instruction executed by the processor on a sequence of clock intervals (cols. 7-10).

As per claims 7-10, Hurd anticipates a FIR filter with coefficients determined to calculate current drawn for power simulation as claimed.

As per claim 11, Hurd anticipates a method and system for determining the power consumption of an integrated circuit with feature limitations very identical to the claimed invention. According to Hurd, the simulation method includes steps

Simulating an operation of the device over a sequence of intervals (col. 7, line 16 to col. 10, line 37),

Determining an activity profile for the device from current drawn by the device in each of the intervals,

Determining response of the power network by applying pulse or impulse stimulus to the network (col. 10, lines 1-25),

And filtering the activity profile with the impulse response of the power delivery network to provide a profile of the voltages at the device (cols. 10-11).

As per claim 12, Hurd anticipates clock gated circuit in a processor under simulation, current pulse in gate circuits to drive the circuit under power simulation, and other logic circuits in support for the processor circuits under simulation.

As per claims 13 and 14, Hurd anticipates step of determining impulse response of the FIR filter including the claimed filter coefficients feature. Hurd also determines pulse response to the current drawn for the power simulation.

As per claim 22, Hurd anticipates a medium on which are stored instructions executable by a computer to implement a method for determining the power consumption of an integrated circuit with feature limitations very identical to the claimed invention. According to Hurd, the computer implemented simulation method includes steps

Art Unit: 2128

Determining a response of a power delivery network including a device under test to a stimulus (col. 7, lines 21-33),

Determining a set of recursion coefficients for the response using FIR design (col. 10, lines 1-25, for example),

Simulating an operation of the device over a sequence of intervals (col. 7, line 16 to col. 10, line 37),

Determining an activity profile for the device from current drawn by the device in each of the intervals,

Determining response of the power network by applying pulse or impulse stimulus to the network (col. 10, lines 1-25),

And filtering the activity profile with the impulse response of the power delivery network to provide a profile of the voltages at the device (cols. 10-11).

As per claim 23, Hurd anticipates the power activity profile generated based on the operation of active or inactive units in the design device, current drawn for active units or inactive units in the execution of a set of simulation instructions, and profiling power consumption in the execution of a set of instructions as claimed.

As per claim 24, Hurd anticipates a FIR filter including the filter order as claimed.

As per claim 25, Hurd anticipates the design including a processor, and the execution of the processor over a set of simulation instructions as claimed.

Allowable Subject Matter

Claims 15-21 are allowed. The following is a statement of reasons for the indication of allowable subject matter: the claimed invention including claims 15-21 is directed to a computer readable medium and method for simulating operation of a processor device to determine 1st through mth current pulses drawn by the device on m successive time intervals, each current pulse being characterized by an amplitude and an offset interval, for each current pulse, scaling the 1st through nth impulse response amplitudes by the amplitude of the current pulse and time-shifting the scaled 1st through nth impulse response amplitudes according to the offset interval to provide 1st through nth scaled impulse response amplitudes in (1+ offset)th through (n+ offset)th intervals, respectively. Because the closest prior art of record does not expressly disclose the claimed features as above for simulating the power consumption induced by current pulses drawn for the processor execution, the claims are thus deemed allowable.

Conclusion

1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
1. US patent no. 4,868,773, issued to Coyle et al, on Sept. 1989
2. US patent no. 5,317,525, issued to Taoka et al, on May 1994
3. US patent no. 6,820,222, issued to Swoboda, Gary, on Nov. 2004

Art Unit: 2128

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 571-272-3783.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on 571-272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

3. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

02/18/05


Thai Phan
Primary Examiner
Art Unit: 2128